SILICON CARBIDE SEMICONDUCTOR DEVICE INCLUDING DEEP LAYER

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is based on and claims priority to Japanese Patent Applications No. 2008-31704 filed on Feb. 13, 2008, No. 2008-322426 filed on Dec. 18, 2008, and No. 2008-322233 filed on Dec. 18, 2008, the contents of which are incorporated in their entirety herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a silicon carbide semiconductor device including a deep layer.

[0004] 2. Description of the Related Art

[0005] A silicon carbide (SiC) semiconductor device typically has a high breakdown field strength and can therefore control a high current. The SiC semiconductor device can be used for controlling a motor of a hybrid vehicle, for example.

[0006] In order to increase electric current that flows in a semiconductor device, a channel density can be increased. In a silicon semiconductor device, a metal-oxide semiconductor field-effect transistor (MOSFET) having a trench gate structure is in practical use. When a trench gate structure is applied to the SiC semiconductor device, difficulty arises. The breakdown field strength of SiC is about ten times greater than a breakdown field strength of silicon. Thus, a voltage about ten times greater than a voltage applied to the silicon semiconductor device may be applied to the SiC semiconductor device. If such a voltage is applied, a gate insulating layer disposed in a plurality of trenches provided in an SiC substrate may receive an electric field about ten times greater than an electric field in the silicon semiconductor device. As a result, the gate insulating layer may be damaged, for example, at a corner portion of each of the trenches. According to a simulation by the inventors named in the present application, when a voltage of about 650 V is applied to a drain, the gate insulating layer in the trenches receives an electric field of about 4.9 MV/cm. The electric filed applied to the gate insulating layer is required to be about 3 MV/cm or less for practical use. Furthermore, the electric filed applied to the gate insulating layer is required to be about 2 MV/cm or less for long-term use.

[0007] In an SiC semiconductor device described in U.S. Pat. No. 5,744,826 (corresponding to JP-A-9-199724), a thickness of an gate insulating layer located at a bottom portion of each of the trenches is set to be greater than a thickness of the gate insulating layer located at a sidewall of each of the trenches for reducing an electric field concentration at the bottom portion of each of the trenches. The SiC semiconductor device described in U.S. Pat. No. 5,744,826 is made of a 4H—SiC substrate having a main surface of (000-1)-face and the trenches extend in a (1120)-direction. An oxidation rate of the (000-1)-face is about five times greater than an oxidation rate of the (1120)-face. Thus, when a gate insulation layer is formed by thermal oxidation in the trenches that have a sidewall of (1120)-face and a bottom of (000-1)-face, a thickness of an oxide layer formed at the bottom portion can be about five times greater than a thickness of the oxide layer formed on the sidewall. Thereby, the electric field concentration at the bottom portion of the trenches can be reduced.

[0008] According to another simulation by the inventors, in which a thickness of the gate insulating layer on the sidewall is set to be about 40 nm and the thickness of gate insulation layer at the bottom portion is set to be about 200 nm, when a voltage of about 650 V is applied to a drain, the electric field concentration at the gate insulating layer in the trenches can be reduced to about 3.9 MV/cm. However, further relaxation of the electric field is required.

[0009] Japanese Patent Application No. 2007-288545 made by the inventors describes an SiC semiconductor device including P type deep layers formed along a longitudinal direction of a trench gate. The P type deep layers are located on an opposite side of an N+ type source region and a P type base region from the trench gate. The P type deep layers are located under a P+ type contact region for electrically coupling the P type base region and a source electrode. The P type deep layers extend to a depth deeper than a bottom portion of the trench gate. In the SiC semiconductor device described therein, the electric field can be further relaxed.

[0010] In a manufacturing process of the above-described SiC semiconductor device, the trench gate and the P type deep layers are formed during different processes. Thus, a positioning is difficult, and a distance between a sidewall of the trench and the P type deep layer may vary. As a result, a production property may vary and a yield may be reduced.

SUMMARY OF THE INVENTION

[0011] In view of the foregoing problems, it is an object of the present invention to provide an SiC semiconductor device including a deep layer.

[0012] An SiC semiconductor device according to a first aspect of the present invention includes a substrate, a drift layer, a trench, a gate insulating layer, a base region, a channel layer, a source region, a gate electrode, a source electrode, a drain electrode, and a deep layer. The substrate is made of silicon carbide and has one of a first conductivity type and a second conductivity type. The substrate has first and second opposing surfaces. The drift layer is located on the first surface of the substrate. The drift layer is made of silicon carbide. The drift layer has the first conductivity type and has an impurity concentration less than an impurity concentration of the substrate. The trench is provided from a surface of the drift layer. The gate insulating layer is located in the trench. The base region sandwiches the trench. The base region has a predetermined distance from the gate insulating layer on a sidewall of the trench. The base region is made of silicon carbide and has the second conductivity type. The channel layer is located between the base region and the gate insulating layer. The channel layer is made of silicon carbide and has the first conductivity type. The source region is located on the base region and sandwiches the trench. The source region is in contact with the channel layer. The source region is made of silicon carbide. The source region has the first conductive type and has an impurity concentration greater than the impurity concentration of the drift layer. The gate electrode is located on the gate insulating layer in the trench. The source electrode is electrically coupled with the source region and the base region. The drain electrode is located on the second surface of the substrate. The deep layer is located under the base region and extends to a depth deeper than the trench. The deep layer is formed along an approximately normal direction to the sidewall of the trench. The deep layer has the second conductivity type. An accumulation channel is provided at the channel layer on the sidewall of the trench and electric current